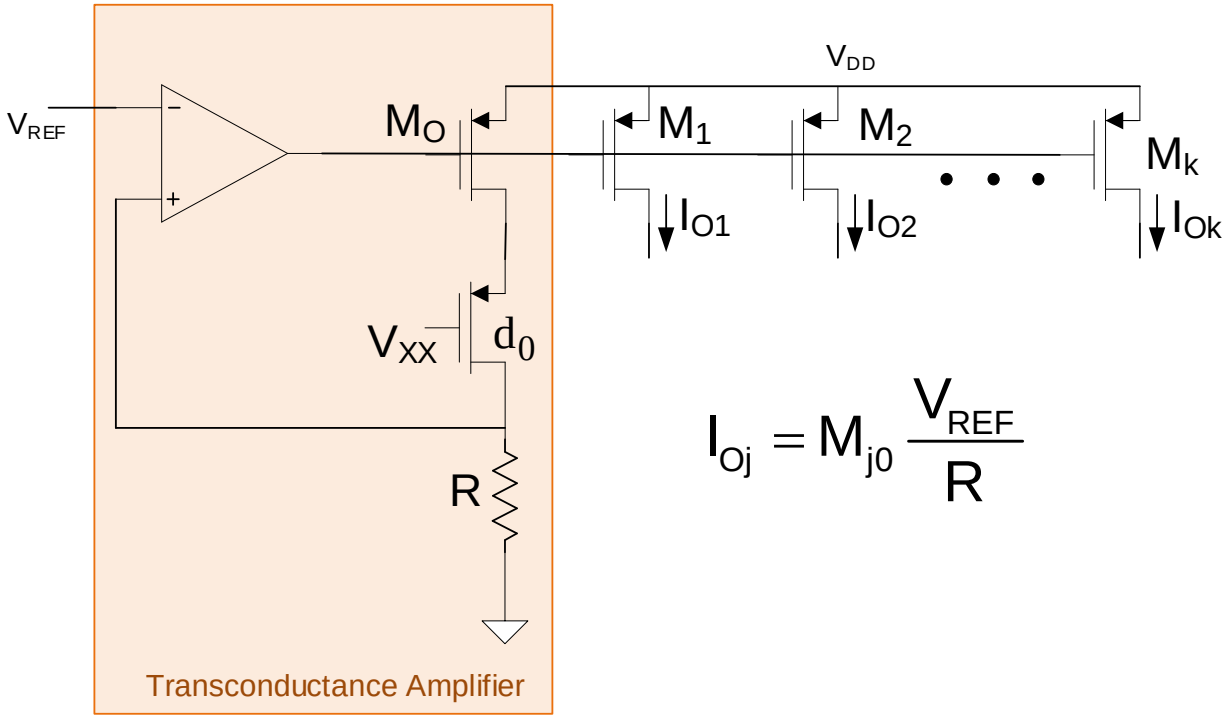
EE 435

Lecture 35

ADC Design

Multiple-output Transconductance Amplifier

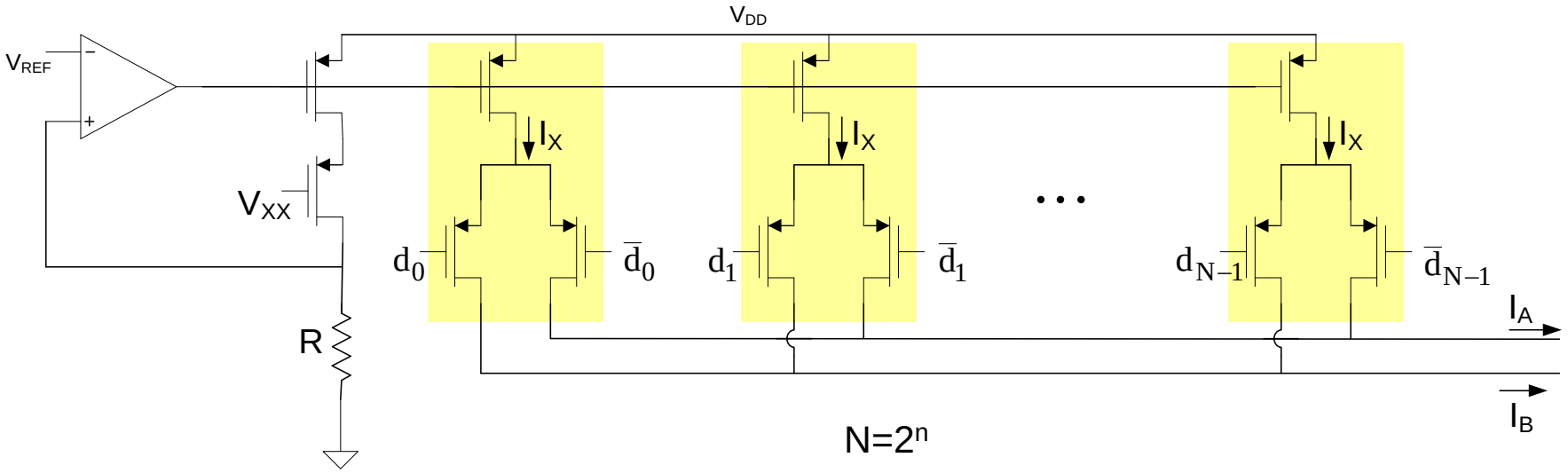


$$I_{Oj} = M_{j0} \frac{V_{REF}}{R}$$

- Good linearity
- Each additional output requires only one additional transistor

Review from Last Lecture

Current Steering DAC with Supply Independent Biasing



If transistors on top row are all matched, $I_X=V_{REF}/R$

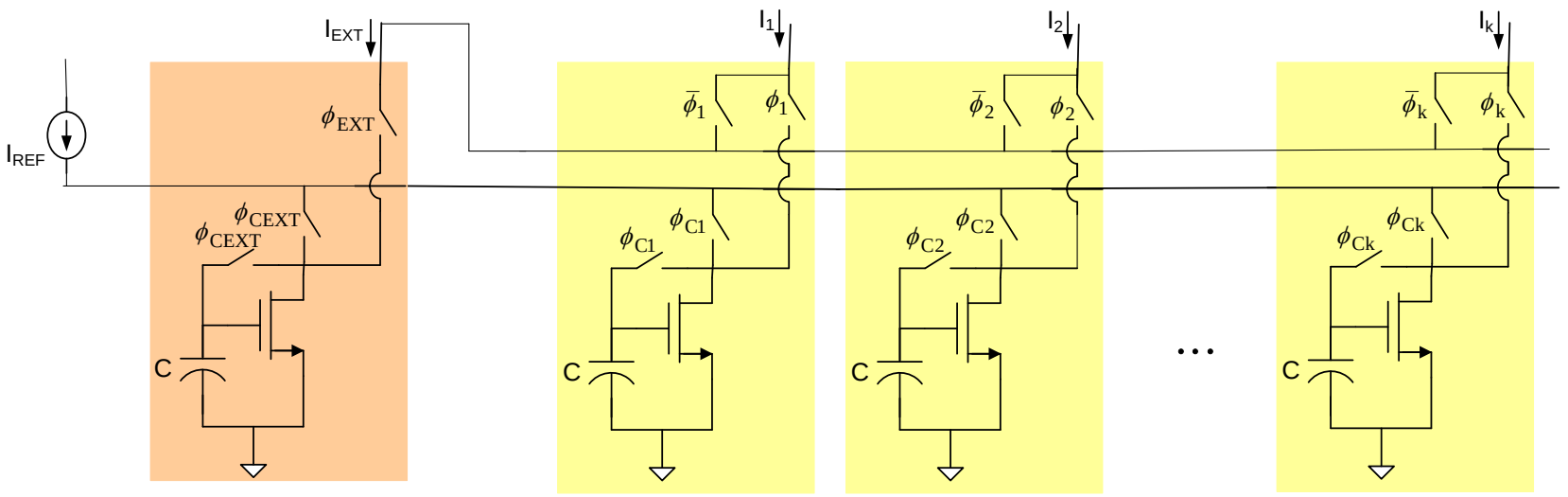
Thermometer coded structure (requires binary to thermometer decoder)

$$I_A = \left(\frac{V_{REF}}{R}\right)\sum_{i=0}^{N-1} d_i$$

Provides Differential Output Currents

Review from Last Lecture

Dynamic Current Source Matching



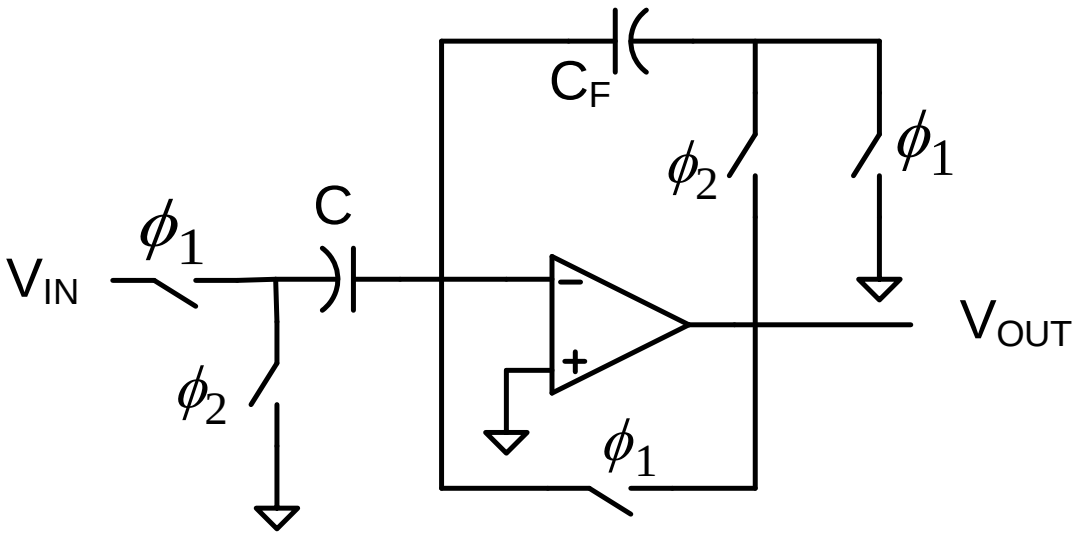
Extra current source can be added to facilitate background calibration

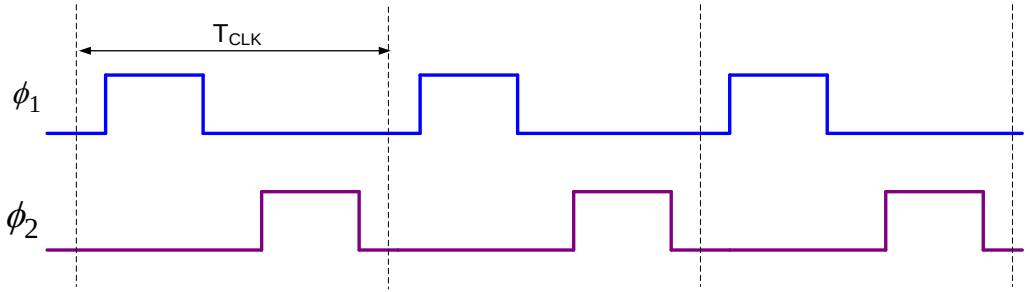
Charge Redistribution DACs

- Previous DACs based upon matching of resistors or transistors
- Switch impedance was of concern in most of the structures
- Capacitor matching can be very good in most processes and area required for a given level of matching may be smaller for capacitors than for resistors or transistors in some processes
- Capacitor linearity is often excellent

Will now focus on building DACs that take advantage of good capacitor matching and linearity

A charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase φ_2

$$\frac{Q_{\phi 1}}{C_F} = V_{OUT}$$

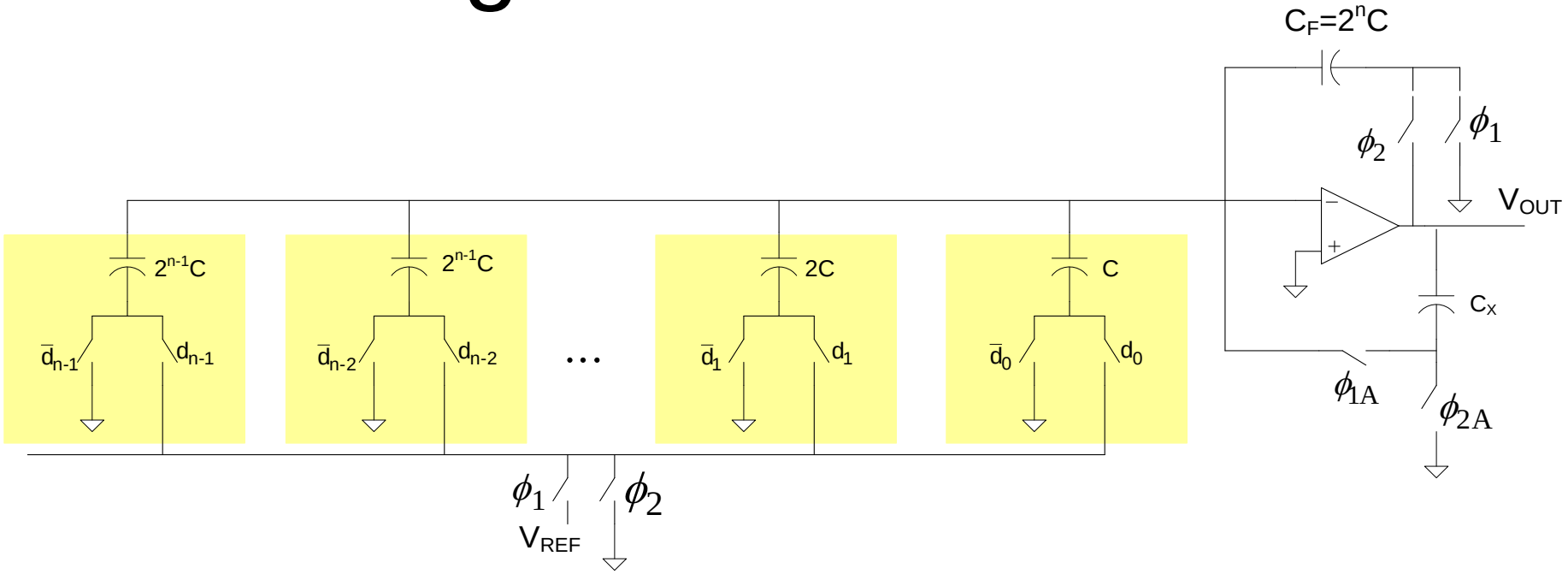
$$\frac{CV_{IN}}{C_F} = V_{OUT}$$

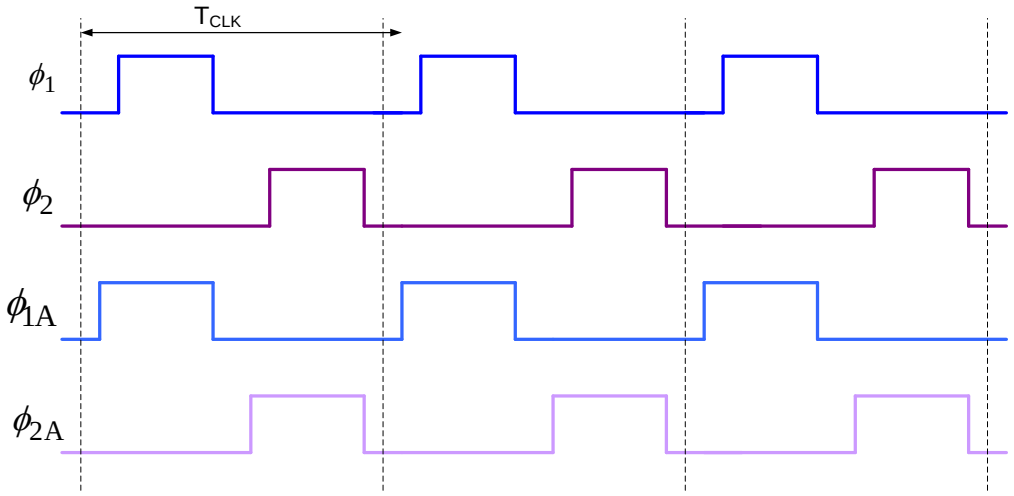
$$\frac{V_{OUT}}{V_{IN}} = \frac{C}{C_F}$$

Serves as a noninverting amplifier
Gain can be very accurate
Output valid only during Φ_2

Review from Last Lecture

A charge redistribution DAC

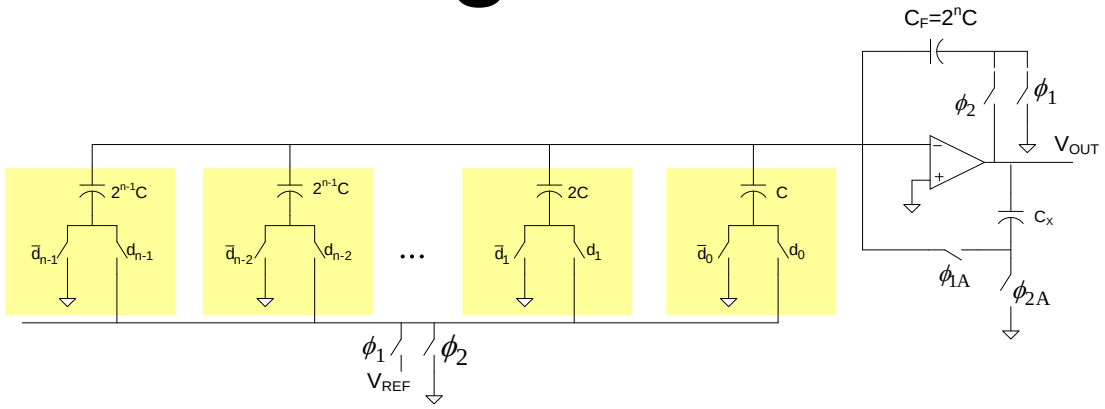


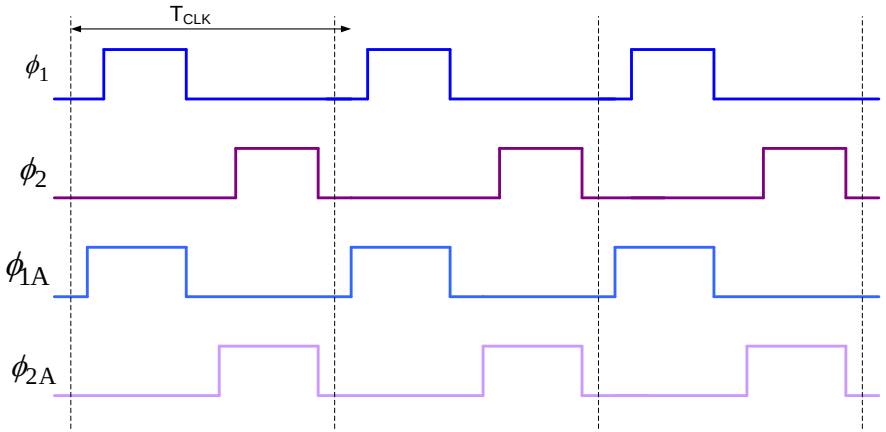


C_X does some good things
(mitigates V_{OS}, 1/f noise and finite gain errors)

Will not consider CX affects at this time

A charge redistribution DAC





During phase φ_1

$$Q_{\phi 1} = V_{REF} \sum_{i=0}^{n-1} d_i \bullet 2^i C$$

$$Q_{CF} = 0$$

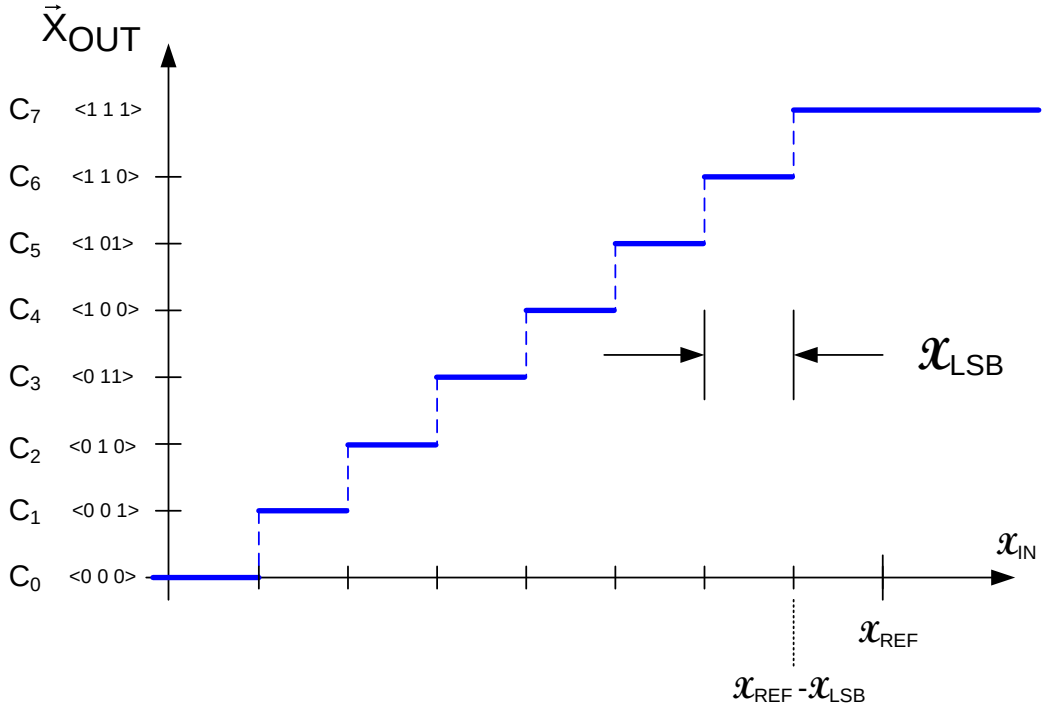
During phase φ_2

$$V_{OUT}(\phi_2) = \frac{1}{C_F} Q_{\phi 1}$$

$$V_{OUT}(\phi_2) = \frac{1}{2^n C} V_{REF} \sum_{i=0}^{n-1} d_i \bullet 2^i C$$

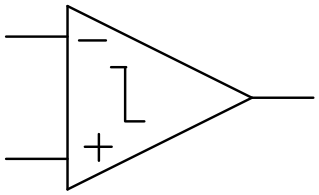
$$V_{OUT}(\phi_2) = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

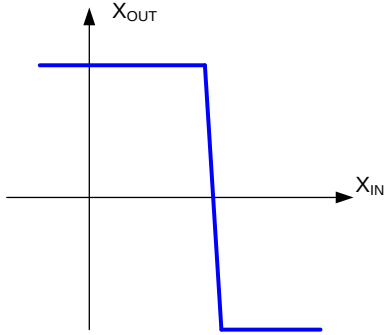
Analog to Digital Converters



Analog to Digital Converters

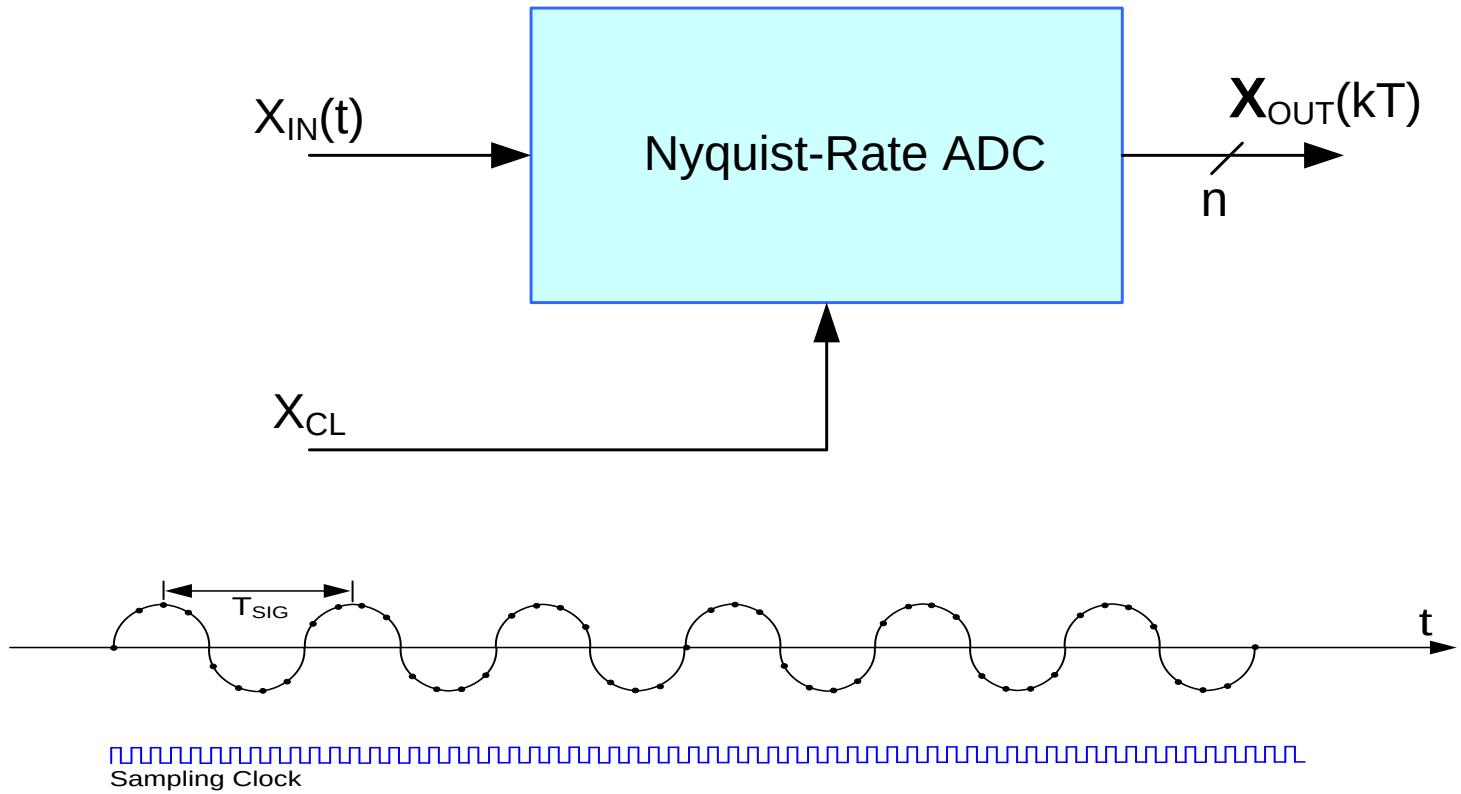
The conversion from analog to digital in ALL ADCs is done with comparators



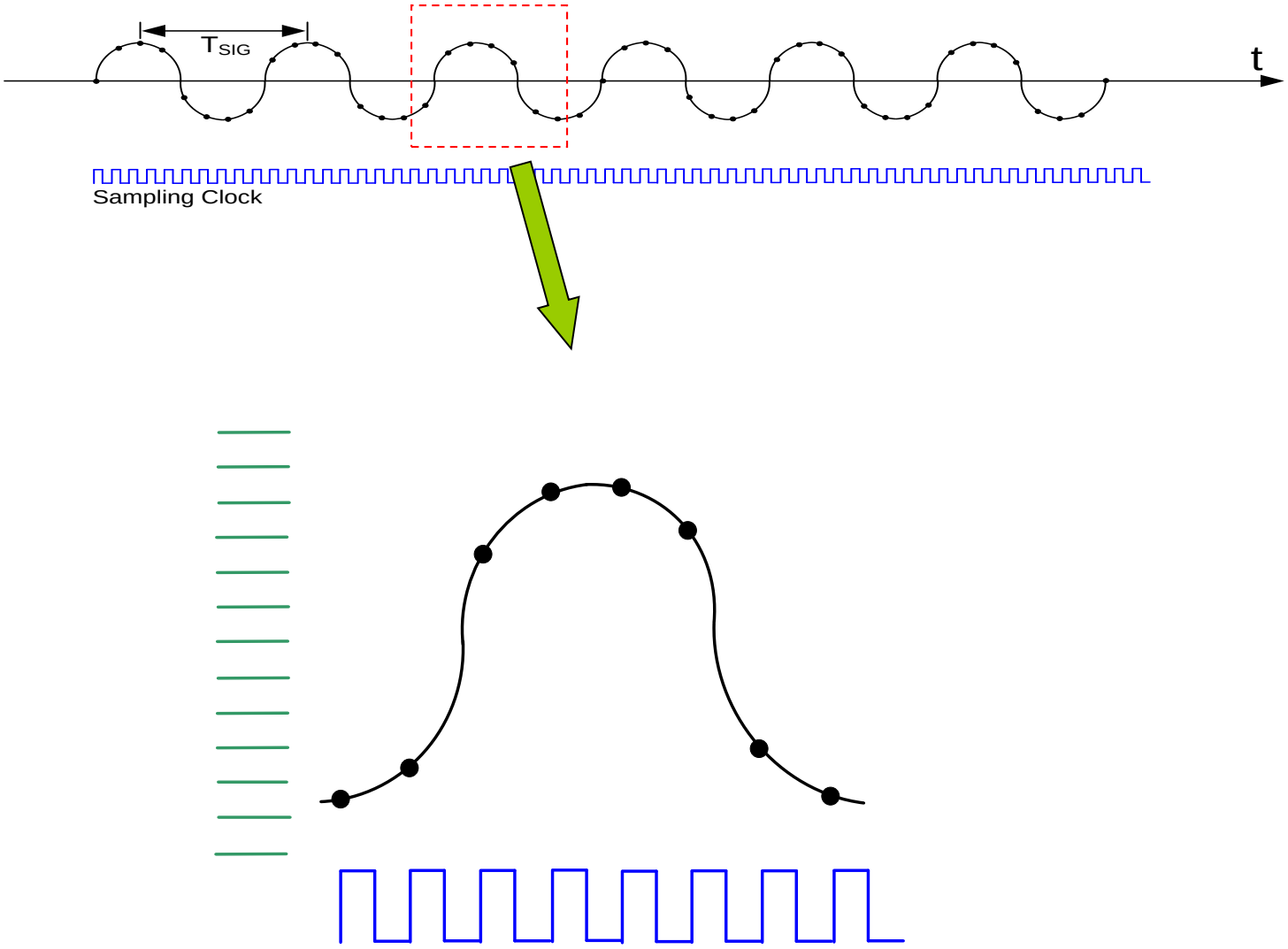


ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects

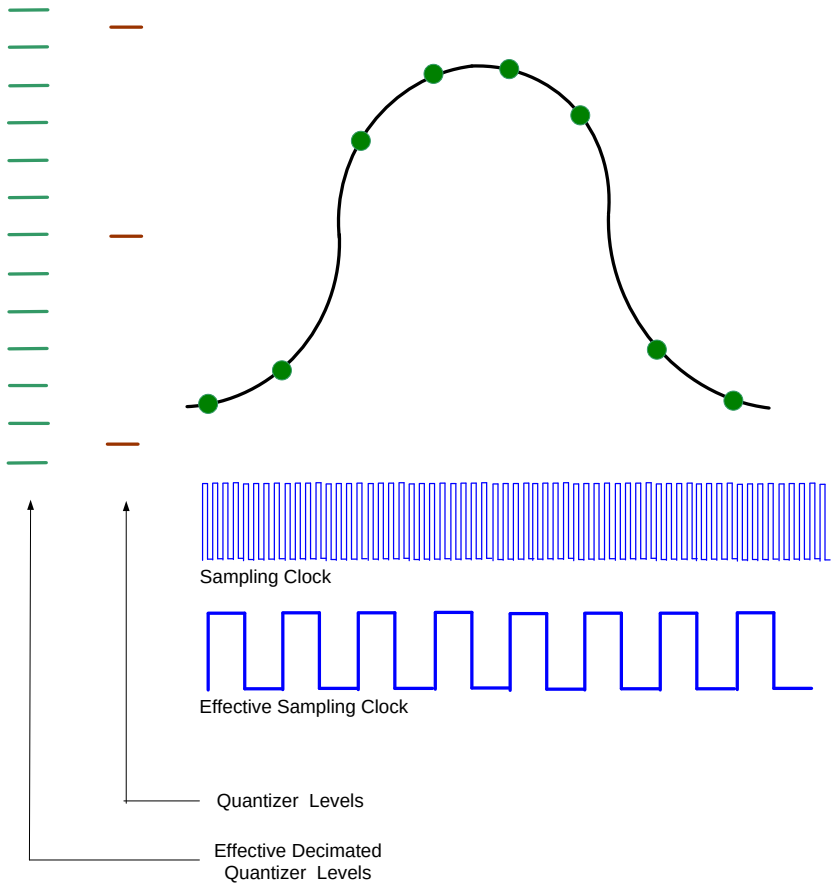
Nyquist Rate



Nyquist Rate

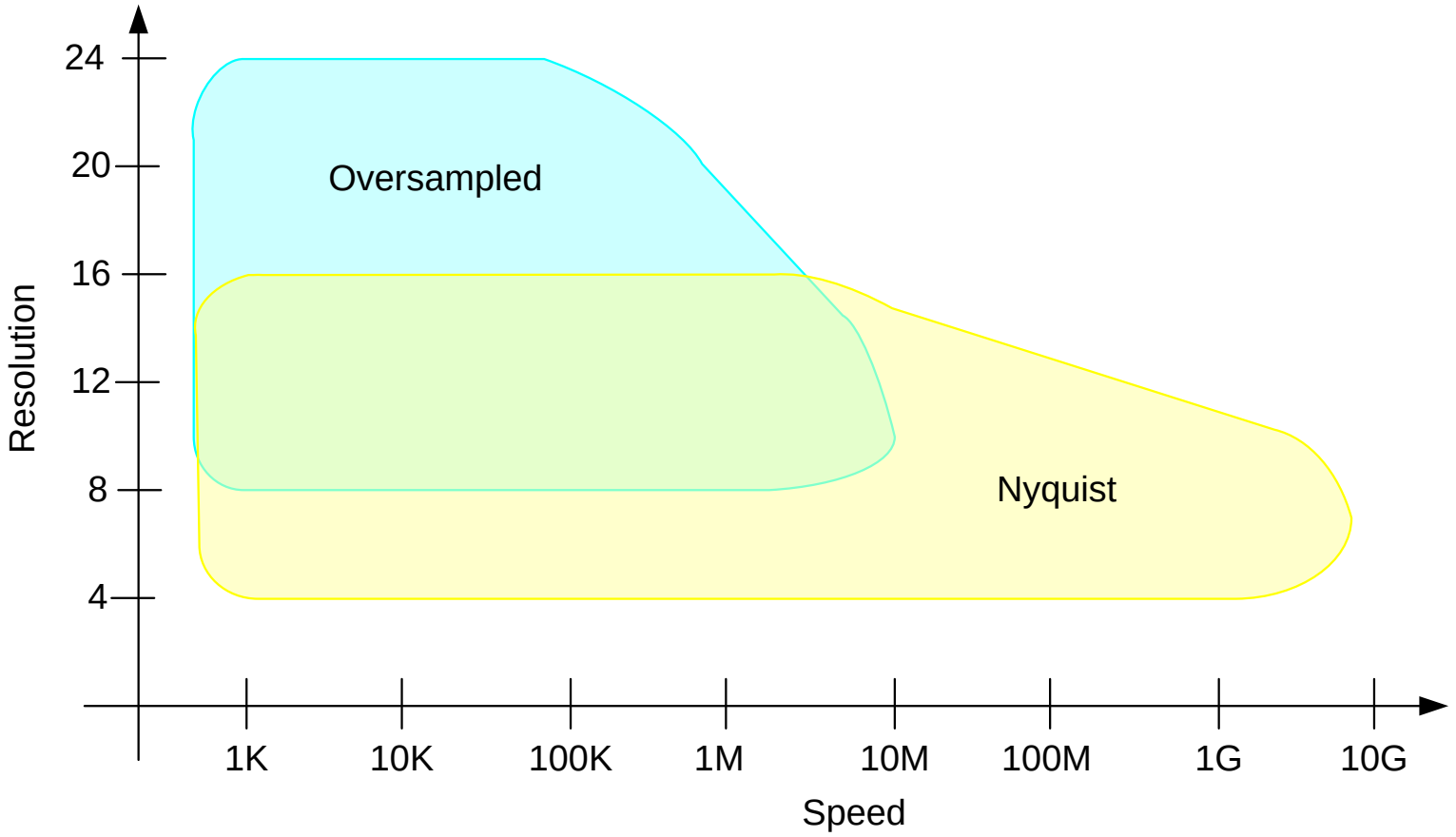


Over-Sampled



Over-sampling ratios of 128:1 or 64:1 are common
Dramatic reduction in quantization noise effects
Limited to relatively low frequencies

Data Converter Type Chart



ADC Types

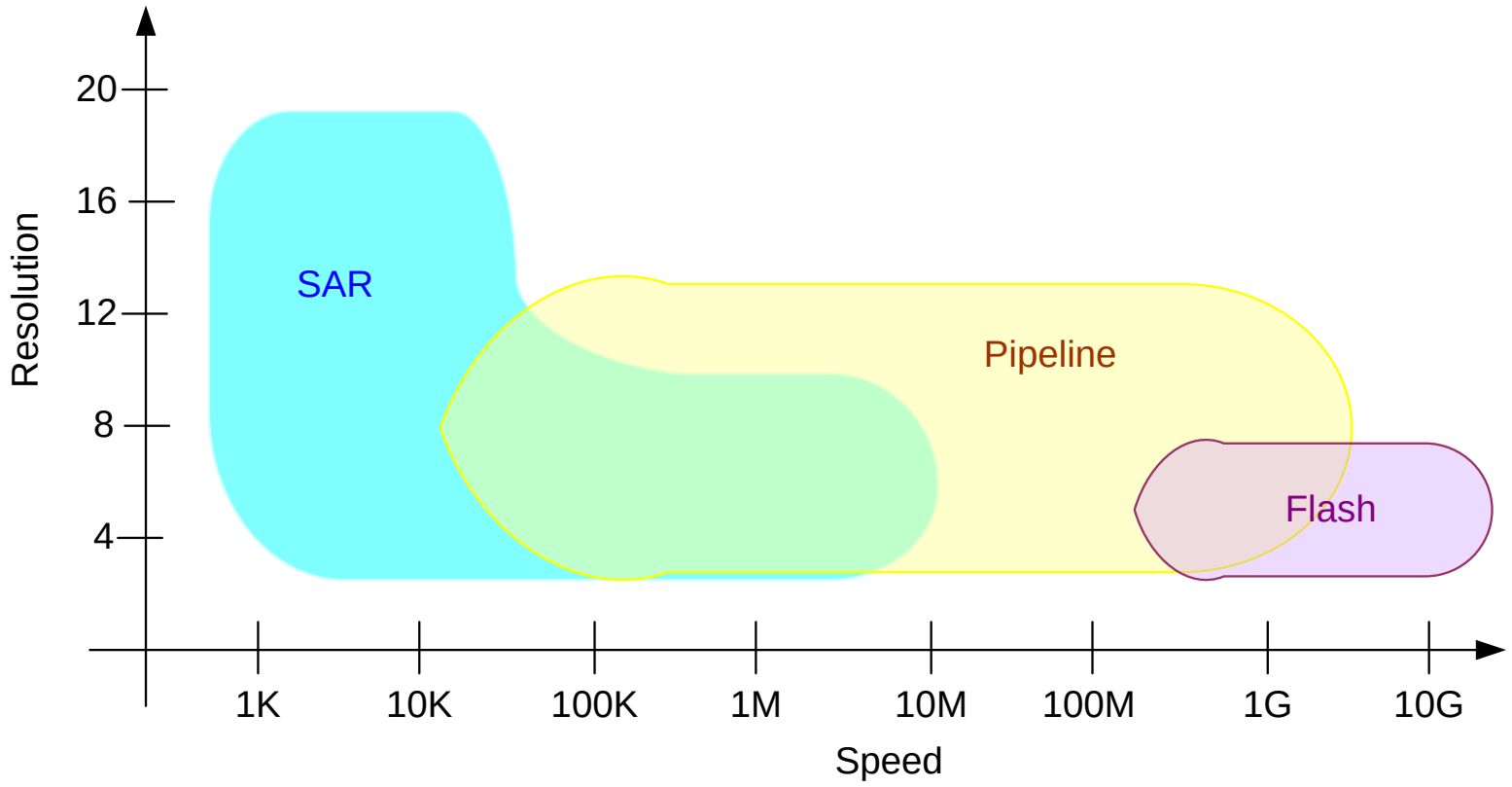
Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

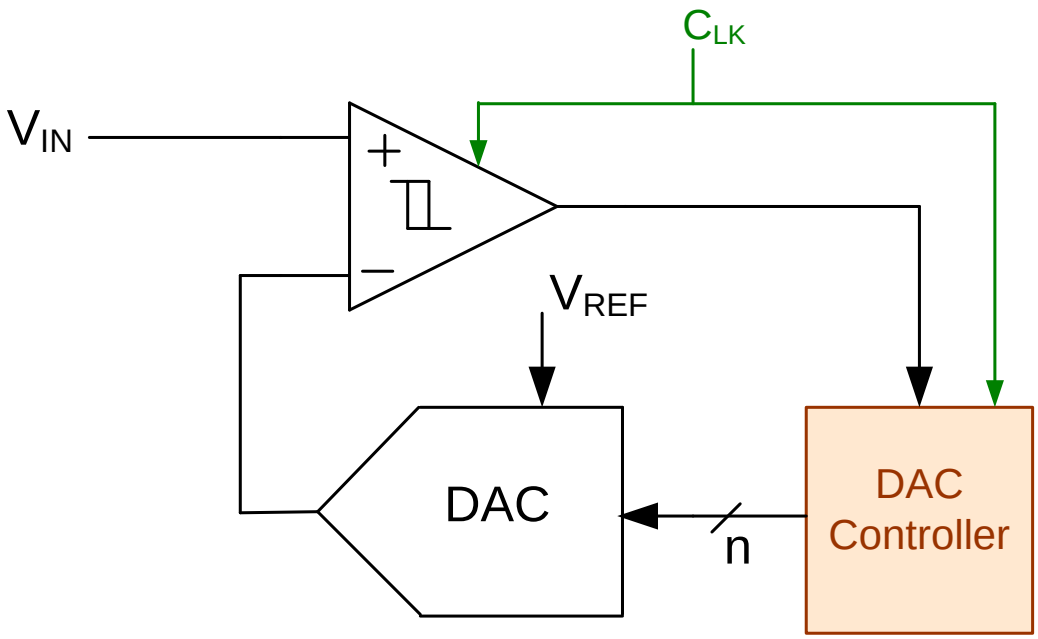
Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

Nyqyist Rate Usage Structures



SAR ADC



- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small

ADC Types

Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

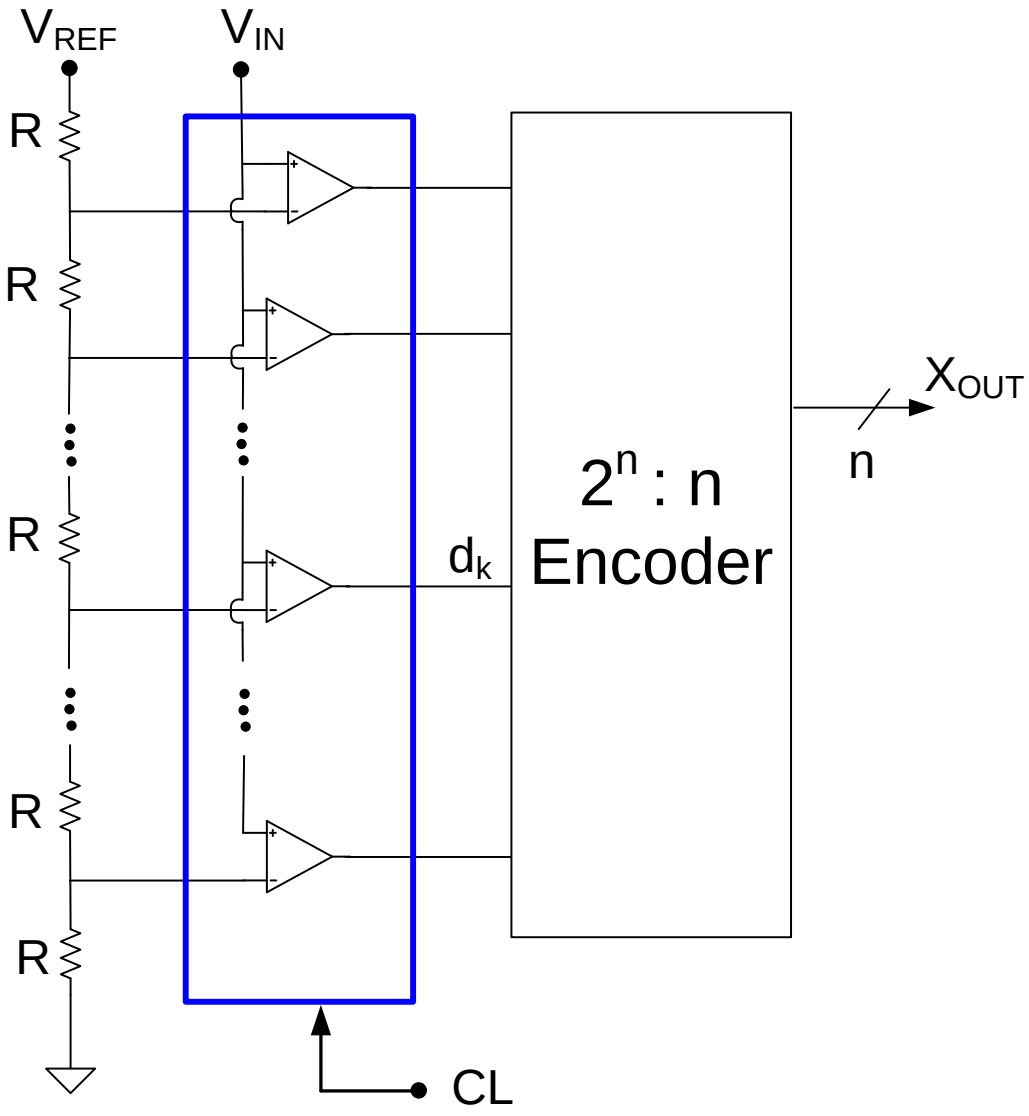
Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

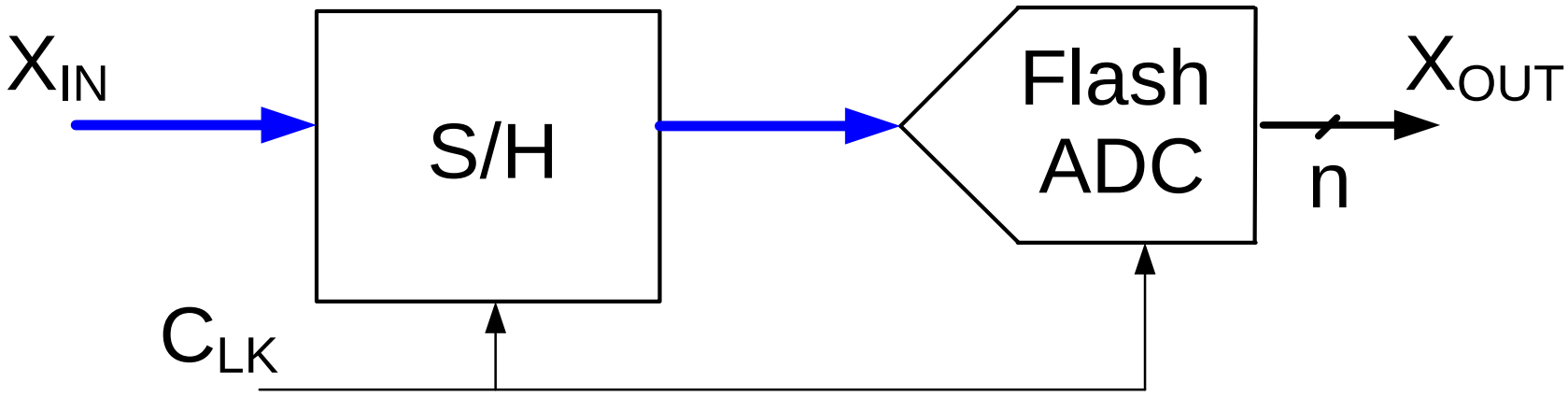
All have comparable conversion rates

Basic approach in all is very similar

Flash ADC



Flash ADC with Front-End S/H



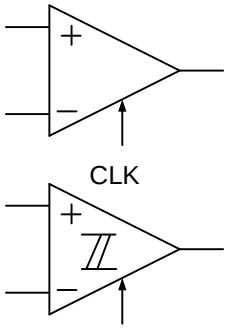
Comparators

High-Gain Saturating Amplifier

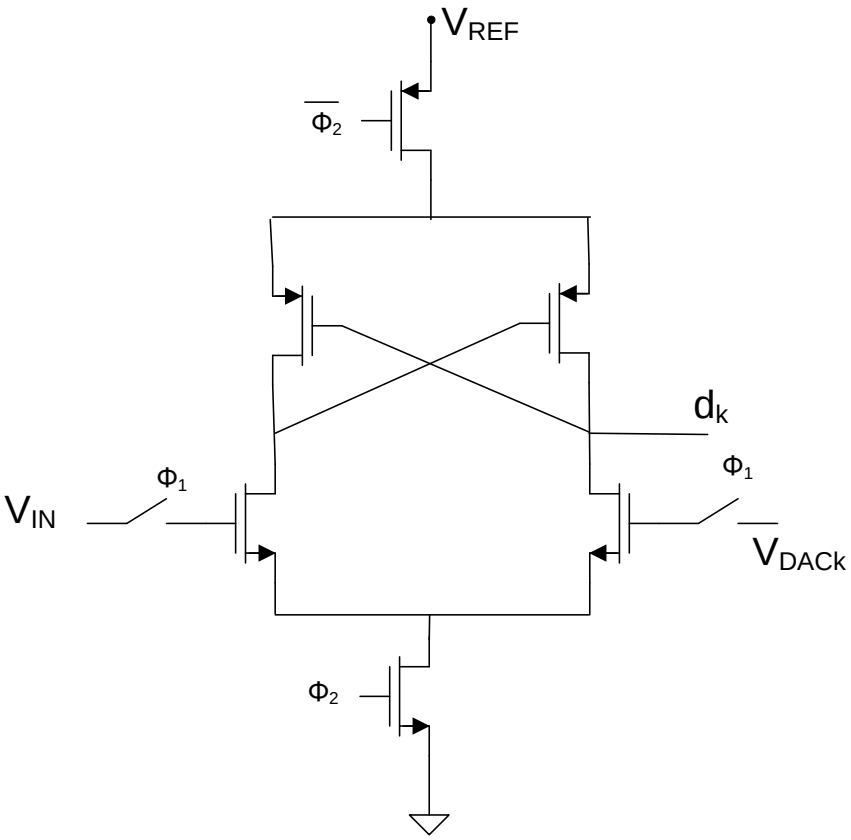
Clocked Comparator

Linear High-gain Amplifier

Regenerative Feedback Amplifier



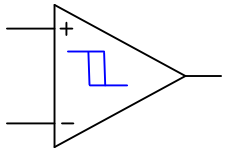
Clocked Comparator



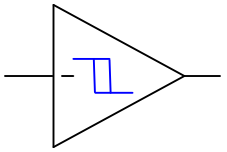
Regenerative Feedback

Large offset voltage (100mV or more)

Regenerative Comparators



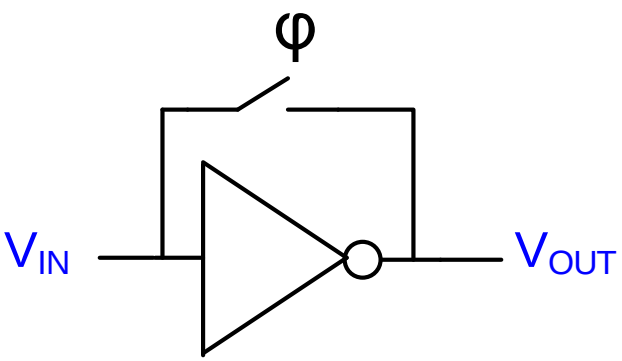
Differential

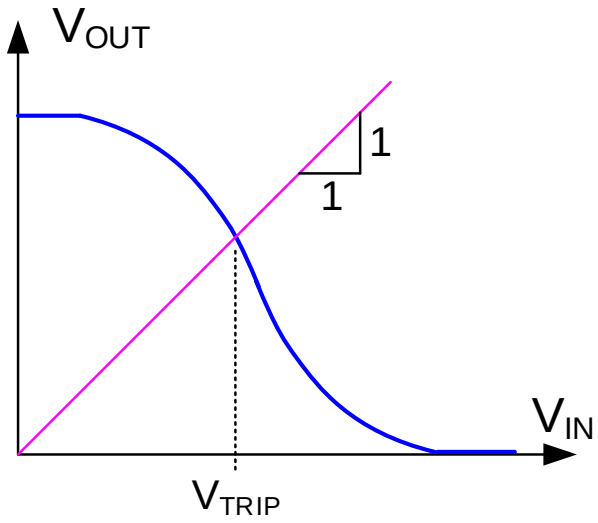


Single-Ended

Clocked Comparator

Recall:



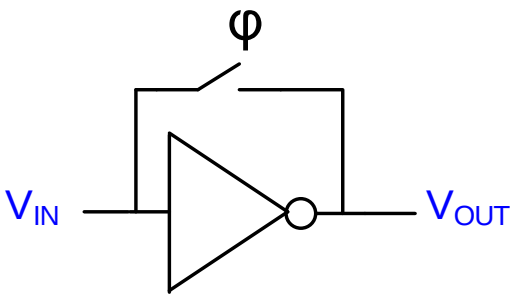


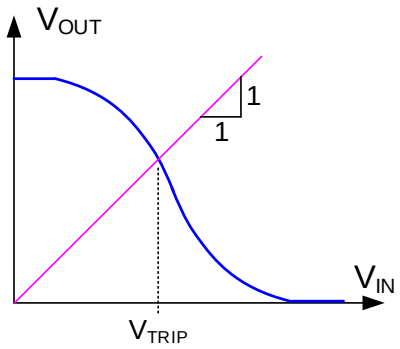
Forcing $V_{OUT}=V_{IN}$ (by closing switch φ) forces the amplifier to operate at the trip point

Concept applicable irrespective of how large the gain of the amplifier is

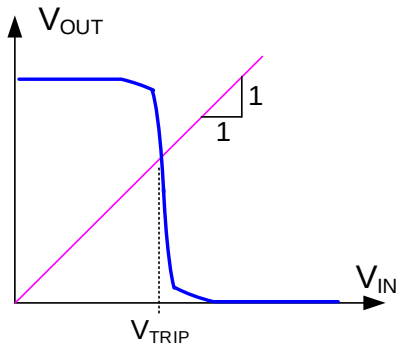
But power dissipation may be high when φ is activated

Clocked Comparator

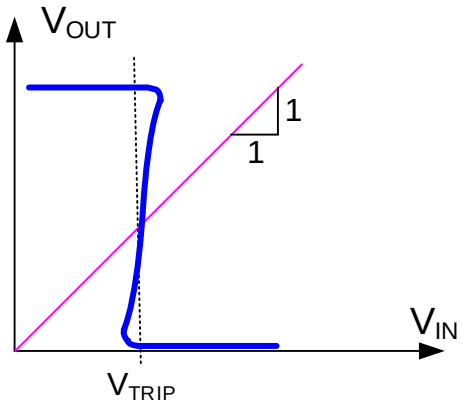




Low Gain Comparator

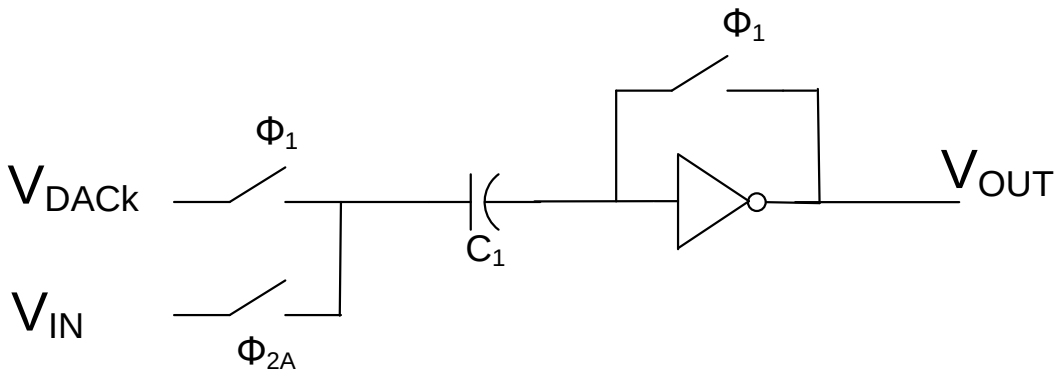


High Gain Comparator



High Gain Comparator with hysteresis (regenerative)

Clocked Comparator



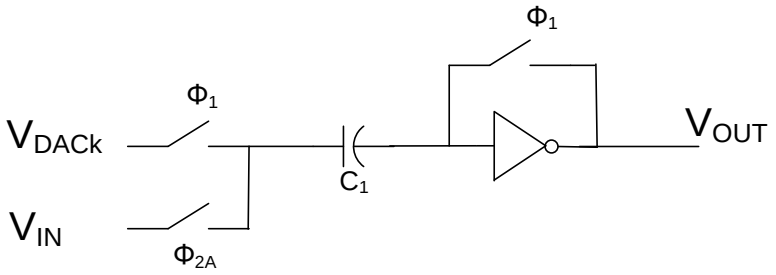
Preamplifier with offset compensation

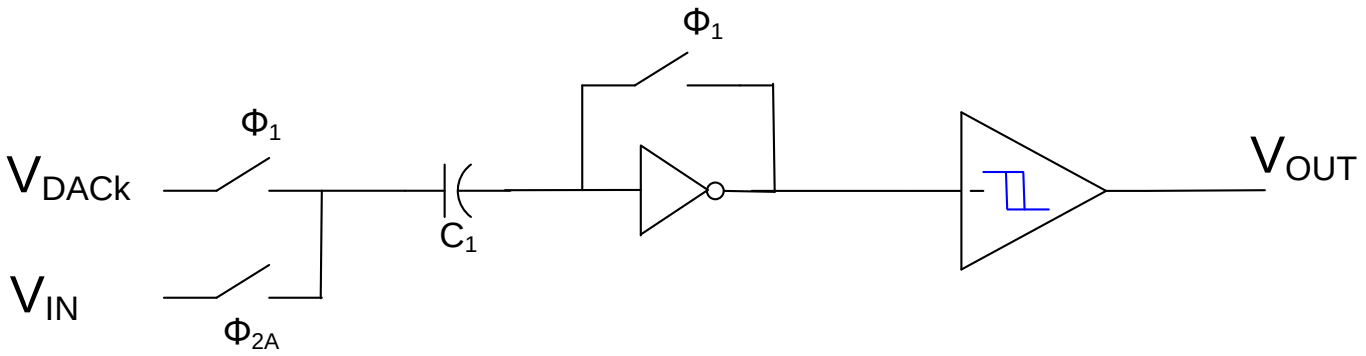
Ideally removes all offset effects

May not have a large enough gain

Regenerative latch often used

Clocked Comparator

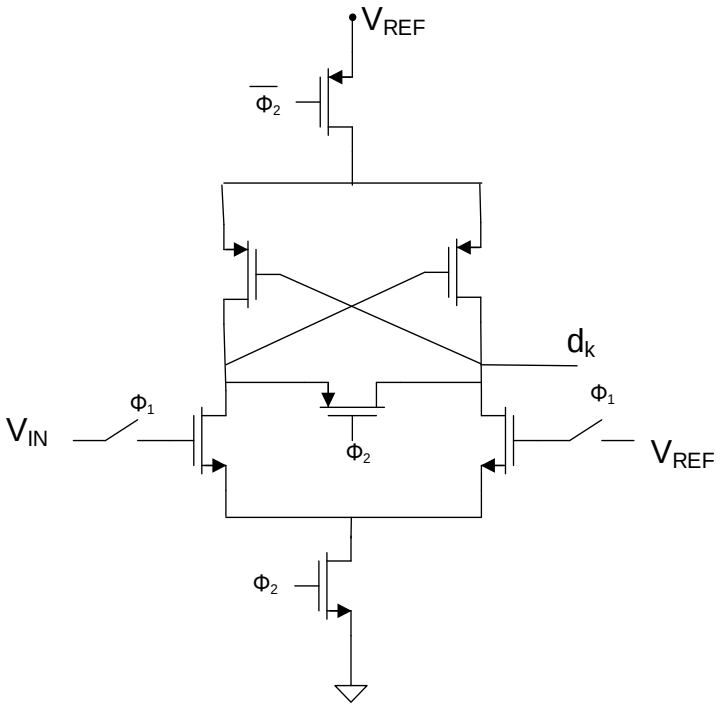




Preamplifier with offset compensation and regenerative latch

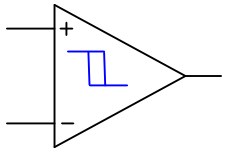
Gain of preamplifier may still not be large enough

Clocked Comparator with Regenerative Feedback

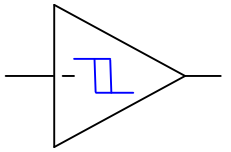


Regenerative Feedback

Regenerative Comparators



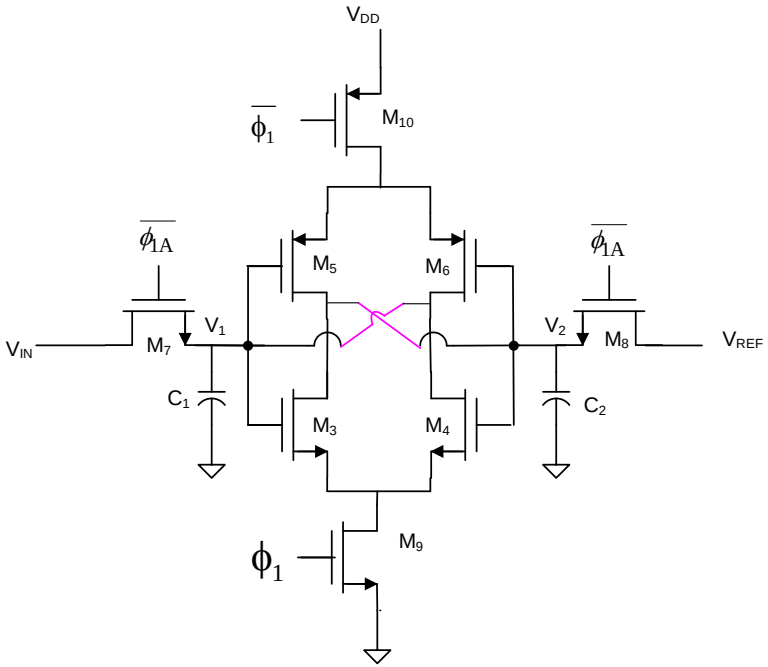
Differential

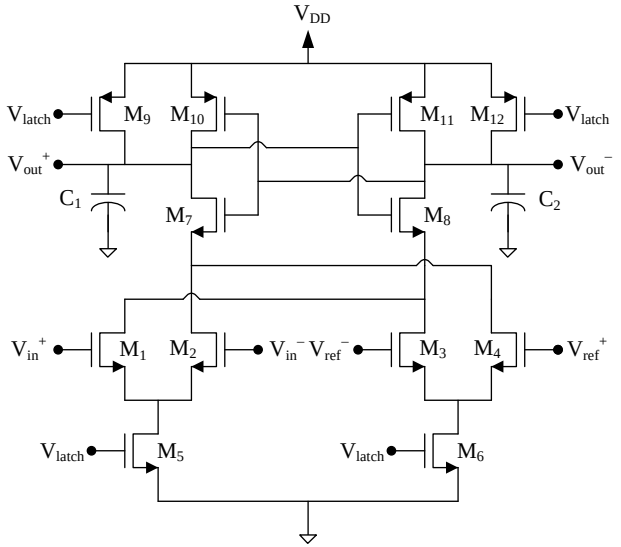


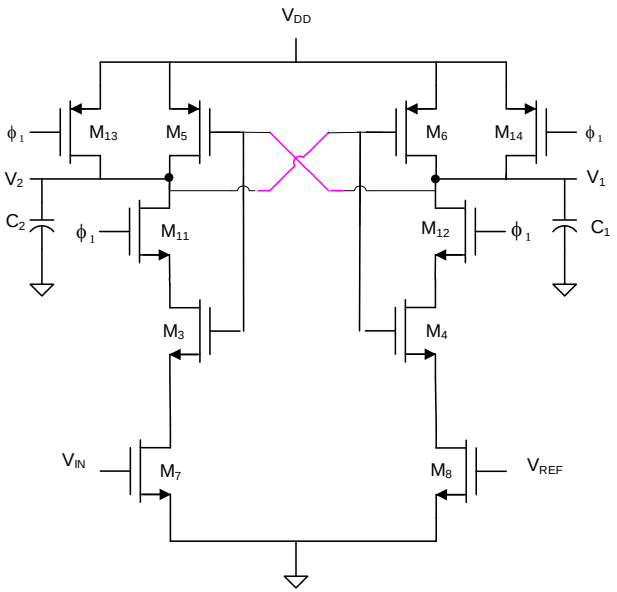
Single-Ended

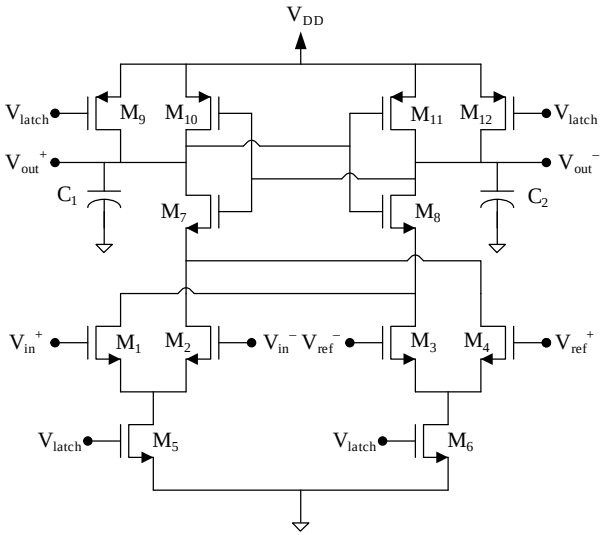
- Regenerative feedback often used to force decision when differential inputs are small
- Several variants of clocked comparators are available
- Important to not have trip point dependent upon previous comparison results
- Often one or more linear gain stages precede the regenerative stage
- Power dissipation can be small in regenerative feedback comparators
- Large offset voltage (100mV or more) common for regenerative feedback comparators

Clocked Comparator with Regenerative Feedback









Flash ADC Summary

Flash ADC

- Very fast
- Simple structure
- Usually Clocked
- Bubble Removal Important
- Seldom over 6 or 7 bits of resolution

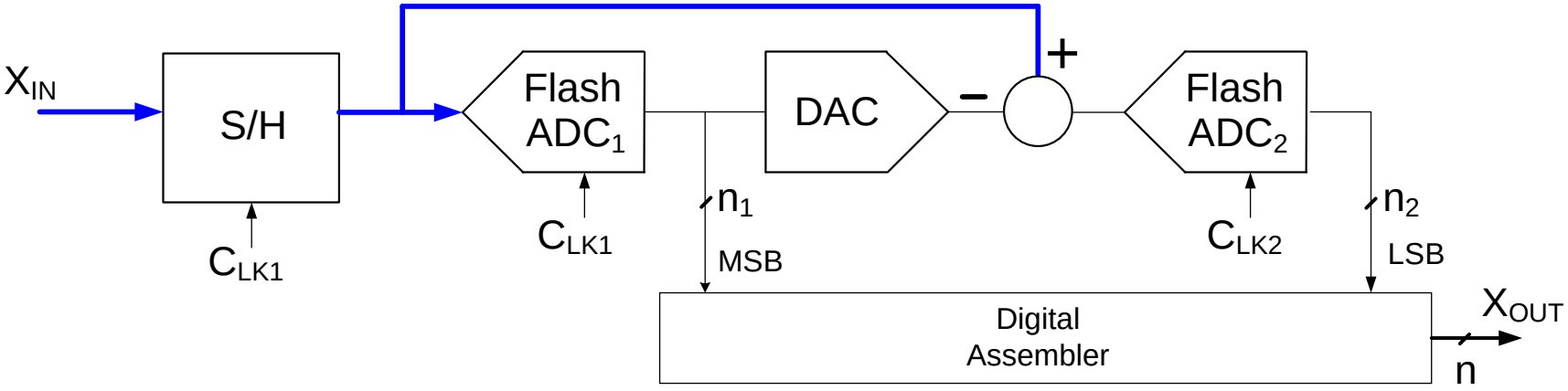
  - Flash ADC has some really desirable properties (simple and fast)
  - Wouldn't it be nice if we could derive most of the benefits of the FLASH ADC without the major limitations

To be practical at higher resolution, must address the major limitation of the FLASH ADC

Major Limitation of FLASH ADC at higher resolutions?

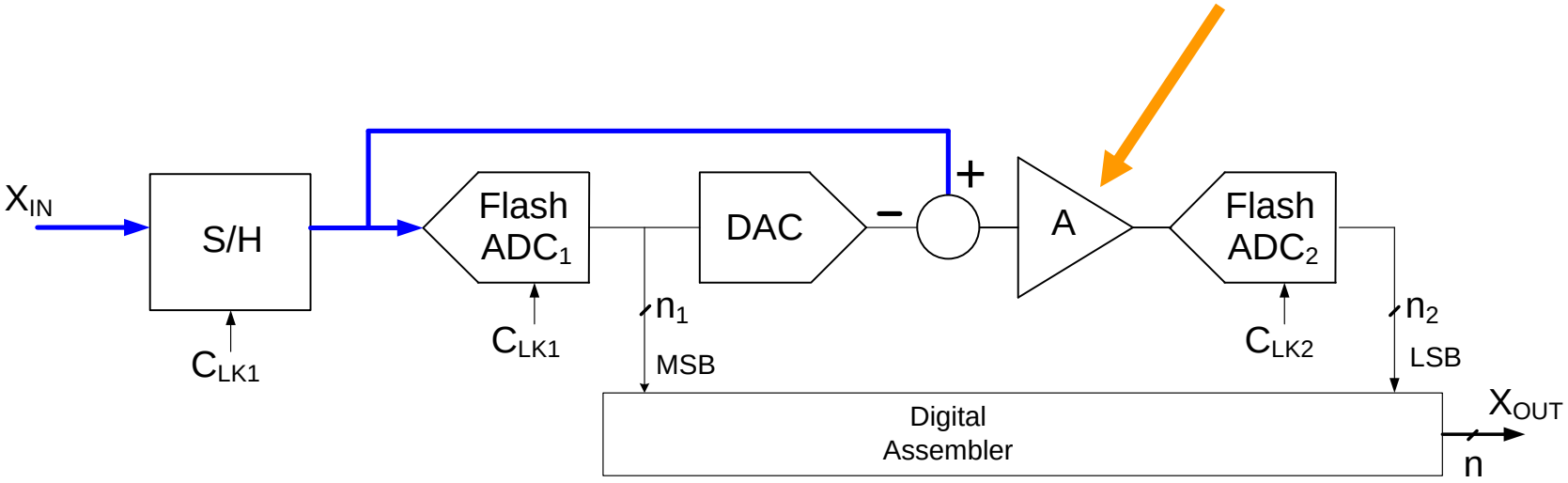
Number of comparators increases geometrically --- 2^n

Two-Step Flash ADC



Can operate asynchronously (either after first S/H or even w/o S/H)

Two-Step Flash ADC with Interstage Gain



Stay Safe and Stay Healthy !

End of Lecture 35